LV11961HA

FAN Motor Driver, Single-phase

ON Semiconductor®
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Overview

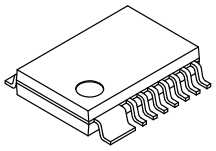
LV11961HA is a driver IC for single-phase fan motor that easily implements direct PWM motor drive system with excellent efficiency. LV11961HA is optimal for fan motor drive in personal computer power supply systems and CPU cooling systems.

Features

- Single-phase full wave drive (built-in power FETs)
- Speed control function by DC voltage input to VTH pin
- Minimum speed adjustment by fixed voltage input to RMI pin
- Soft start-up function by SFS pin
- Regulated voltage output pin for Hall bias
- Built-in lock protector and auto recovery circuit
- FG signal output pin, RD signal output pin
- Built-in TSD (Thermal shutdown) circuit

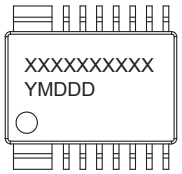
Typical Applications

- Fan motor units
- Note PCs
- Desk top PCs
- Projectors



HSSOP14 (225mil)

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

ORDERING INFORMATION

Ordering Code:
LV11961HA-AH

Package
HSSOP14 (225mil)
(Pb-Free / Halogen Free)

Shipping (Qty / packing)
2000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

Specifications

Absolute Maximum Ratings at Ta = 25°C (Note 1)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	VCCmax		18	V
Output pin current	IOUTmax		1.0	A
Output pin peak current	IOpeak max	Duty ≤ 10%	1.2	A
Output pin with stand voltage	VOUTmax		18	V
REG output maximum current	IREGmax		10	mA
HB output maximum current	IHBmax		10	mA
VTH pin voltage	VTHmax		4	V
FG/RG output pin voltage	VFG/VRDmax		18	V
FG/RG pin sink current	IFG/IRDmax		10	mA
Allowable power dissipation	Pdmax	Mounted on specified board (Note 2)	1.1	W
Operating temperature	Topr	(Note 3)	–40 to +95	°C
Storage temperature	Tstg		–55 to +150	°C

1. Stresses exceeding those listed in the Absolute Maximum Rating table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Specified board: 114.3mm x 76.1mm x 1.6mm, glass epoxy board
3. Do not exceed Tjmax=150°C

Recommendation Operating Condition at Ta = 25°C (Note 4)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply voltage range	VCCop		3.6	12	16	V
VTH pin input voltage range	VTHop		0		VREG	V
RMI pin input voltage range	VRMIop		0		VREG	V
IN1/IN2 pin input voltage range	VICM		0.2		VREG–1.2	V
CPWM pin oscillation frequency range	fCPWM		20		100	kHz

4. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at Ta = 25°C, V_{CC} = 12V (Note 5)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current	ICC			2.0	3.0	mA
REG pin voltage	VREG	IREG=5mA	2.80	3.15	3.50	V
HB pin voltage	VHB	IHB=5mA	1.08	1.2	1.32	V
CPWM pin high threshold level	VCPH		2.05	2.15	2.25	V
CPWM pin low threshold level	VCPL		0.57	0.62	0.67	V
CPWM amplitude	DVCP		1.41	1.53	1.65	V
CPWM pin charge current	ICPWM	VCPWM=1.4V	19	24	32	μA
CPWM pin discharge current	ICPWM	VCPWM=1.4V	–32	–24	–19	μA
SFS pin charge current	ISFS		0.75	1.25	1.85	μA
SFS pin clamp voltage	VSFSCL		0.2	0.4	0.6	V
Sensitivity to hall input	VHIN	Design target (Note 6)		10	20	mV
OUT pin low level voltage	VOL	IOUT=200mA		0.11	0.17	V
OUT pin high level voltage	VOH	IOUT=200mA		0.18	0.27	V
FG/RD pin low level voltage	VFGL/VRDL	IOUT=3mA		0.1	0.2	V
FG/RD pin leak current	IFGL/IRDL	VFG/VRD=18V			10	μA

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Lock detection output ON time	LT1		0.45	0.75	1.05	Sec
Lock detection output OFF time	LT2		4	7	10	Sec
Lock detection ON/OFF ratio	LRTO	LRTO=LT2/LT1	8	9	10	
Thermal shutdown operating temperature	TSD	Design target (Note 6)		180		°C
Thermal shutdown hysteresis width		Design target (Note 6)		30		°C

5. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
6. Design target: These values are the target value in designs. The parameters are not measured independently.

Truth table

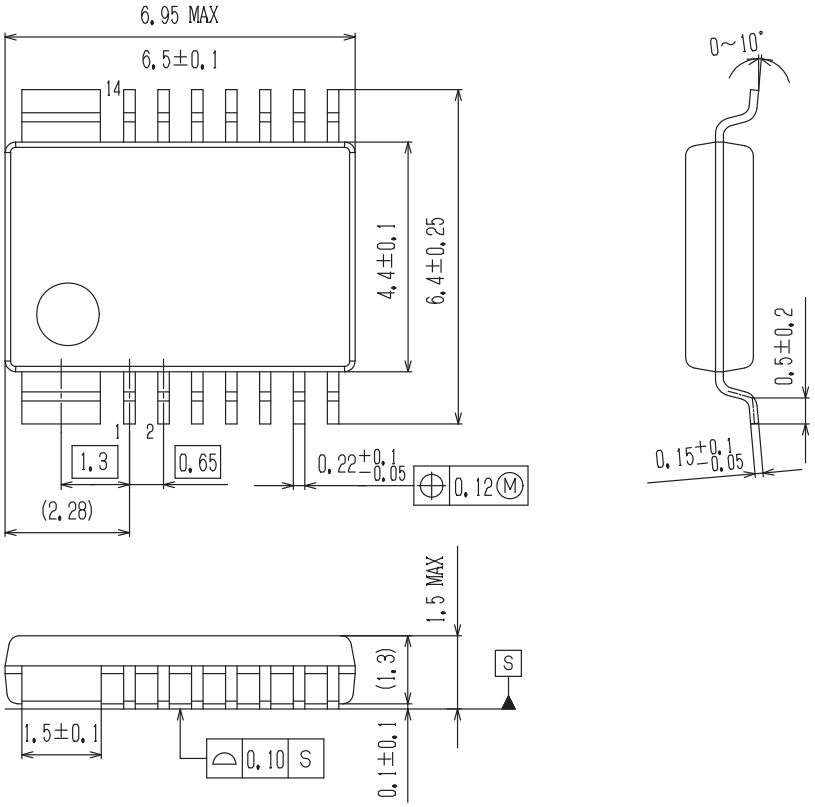
VTH	IN1	IN2	CPWM *1	OUT1	OUT2	FG	RD	Mode
L (OPEN)	L	H	H	H	L	L	ON	Driving
	H	L		L	H	OFF		(PWM-OFF)
H	L	H	L	OFF	L	L		Regenerating
	H	L		L	OFF	OFF		(PWM-ON)
-	L	H	-	H	OFF	L	OFF	Lock protection
-	H	L		OFF	H	OFF		

*1 CPWM=H : CPWM>VTH, CPWM=L : CPWM<VTH

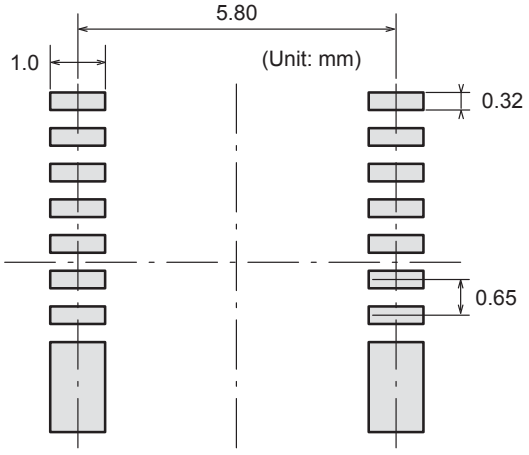
Package Dimensions

unit : mm (typ)

HSSOP14 (225mil)
CASE 944AA
ISSUE A



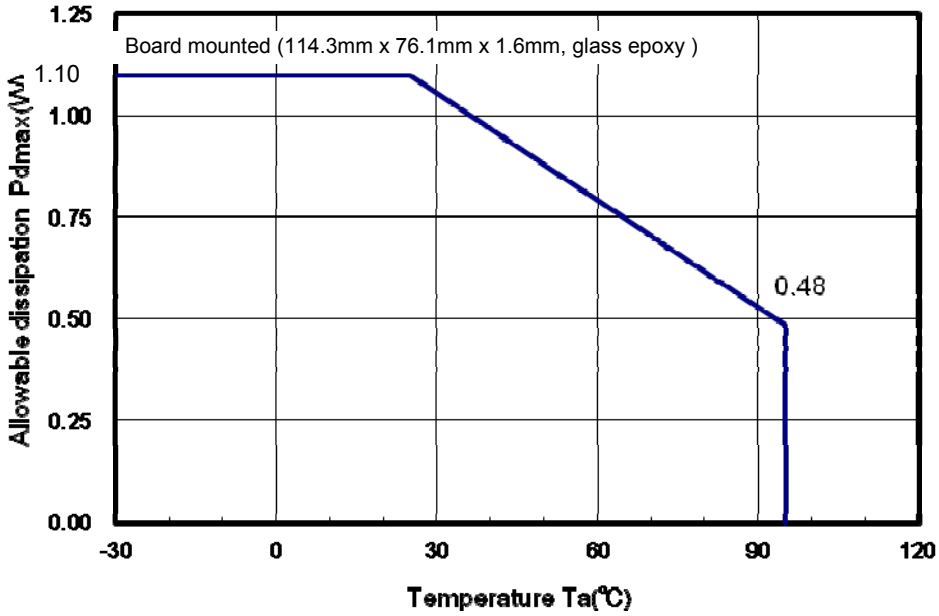
SOLDERING FOOTPRINT*



NOTES: 1. The measurements are not to guarantee but for reference only.
2. Land pattern design in Fin area to be altered in response to customer's individual application.

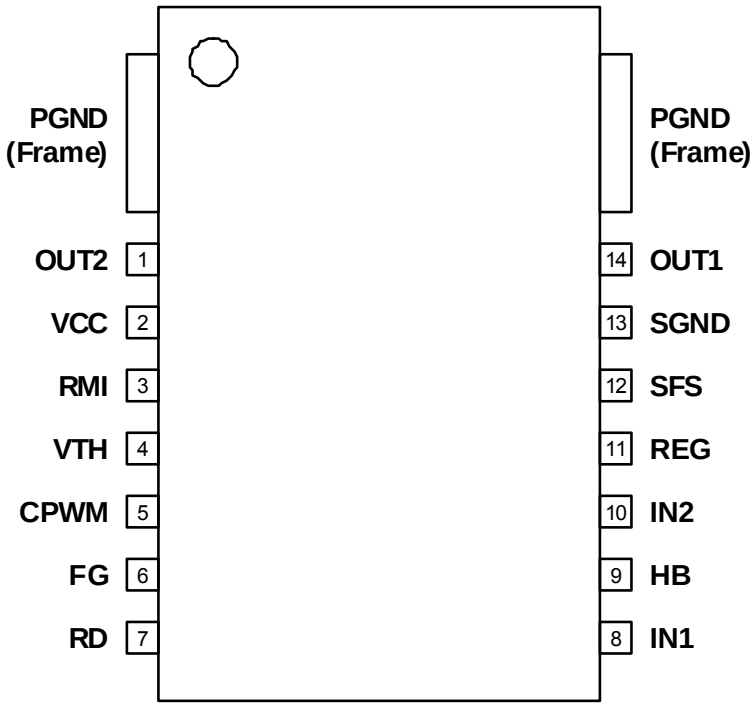
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Pdmax-Ta diagram

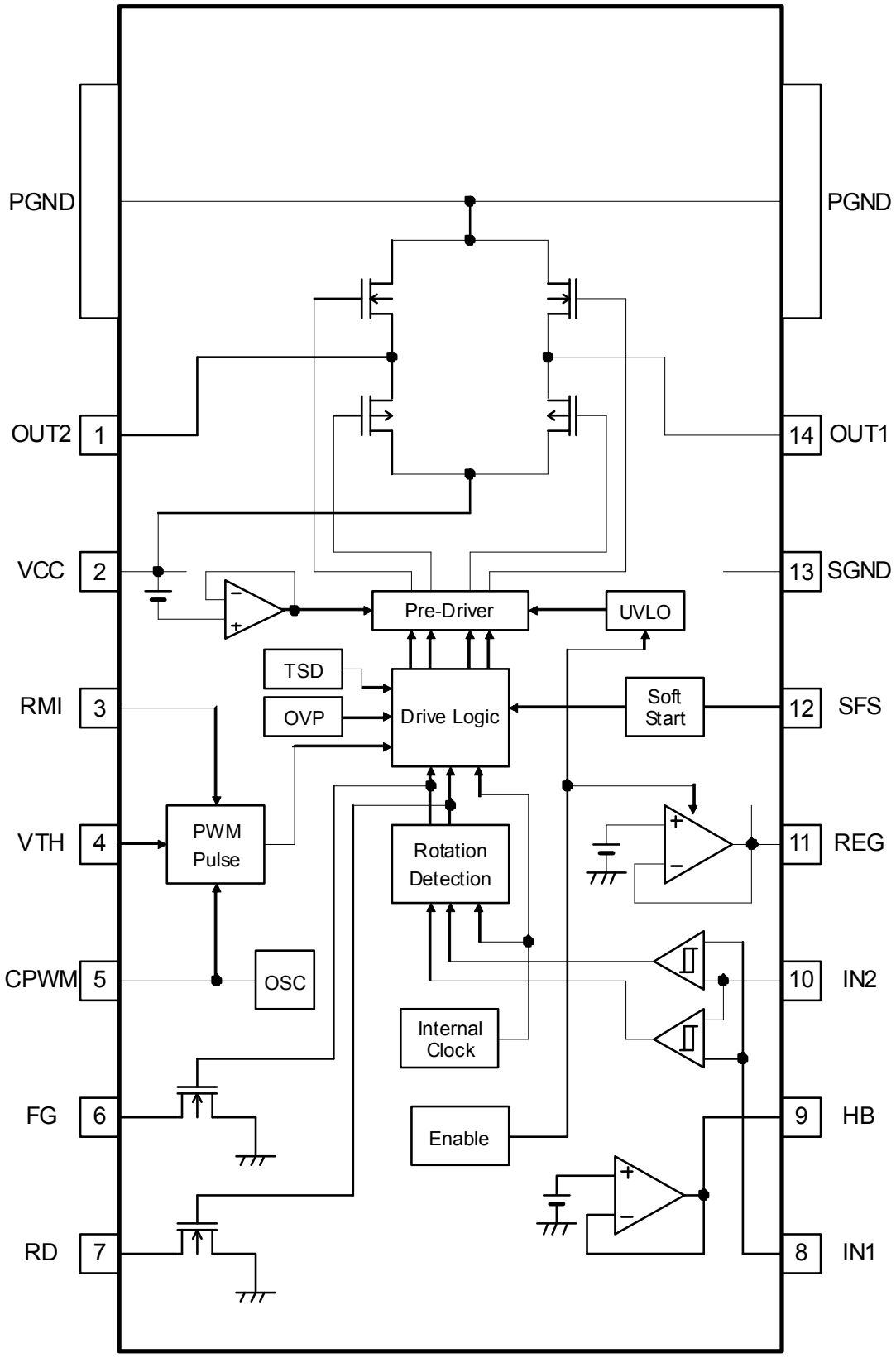


Pin Assignment

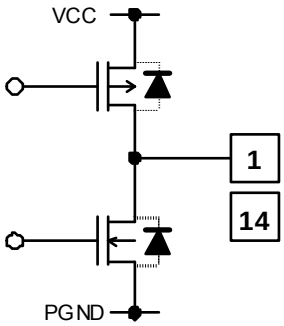
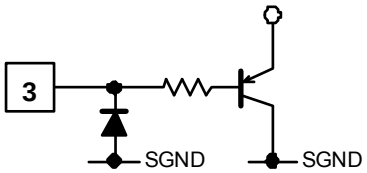
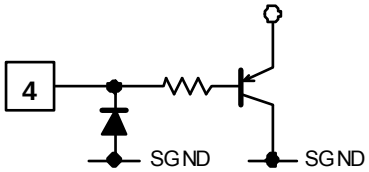
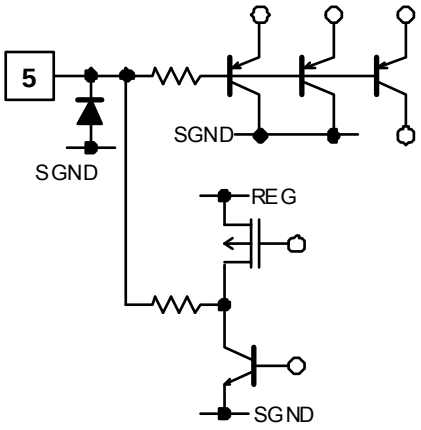
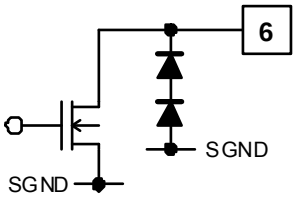
Package: HSSOP14 (225mil)



Block Diagram



Pin function

Pin No.	Name	Function	Equivalent circuit
1	OUT2	Output for motor drive(2).	
14	OUT1	Output for motor drive(1).	
2	VCC	Supply voltage input.	
3	RMI	Input to adjust the minimum duty at PWM.	
4	VTH	Input to control PWM duty.	
5	CPWM	Output of oscillation for PWM.	
6	FG	Output of motor rotational signal.	

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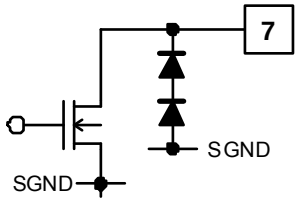
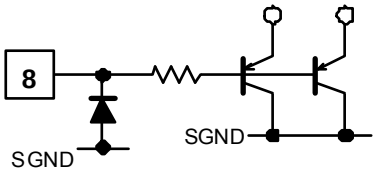
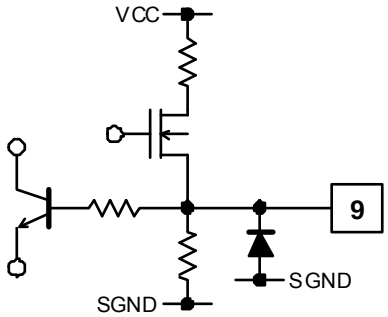
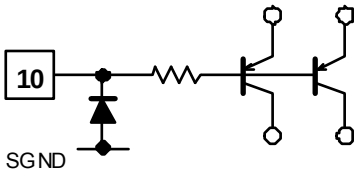
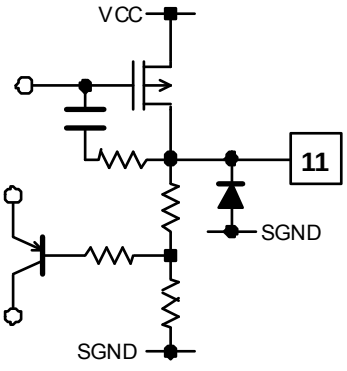
Pin No.	Name	Function	Equivalent circuit
7	RD	Output of motor lock detection.	
8	IN1	Input of hall signal (1).	
9	HB	Output of regulated voltage for hall bias.	
10	IN2	Input of hall signal (2).	
11	REG	Output of regulated voltage (3.2V). This voltage supplies power for internal circuits to control.	

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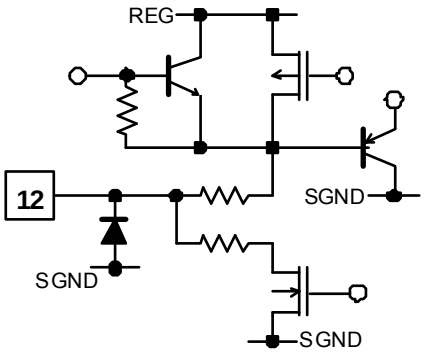
Pin No.	Name	Function	Equivalent circuit
12	SFS	Input to adjust the time of soft starting.	
13	SGND	GND for internal circuits to control.	
Frame	PGMD	GND to power MOSFETs. In addition, these pins contribute for radiation.	

Functional description

- Start Up

In the condition that VTH and RMI level is higher than VCPWM level continuously over 1.5ms (typical), IC is in the sleep mode. Once VTH level is lower than VCPWM level, IC turns to be active and goes into the Start-up mode.

In the Start-up mode, PWM duty of OUT1 and 2 in start-up operation is decided by SFS level.

By connecting a capacitor between SFS pin and SGND, the voltage of SFS pin begins to increase soon after IC booting.

After IC booting, PWM output is in the mode of ...

Driving (under the condition of SFS > CPWM in the charging period of CPWM)

Regenerating (the discharging period of CPWM and under the condition of SFS < CPWM in the charging period of CPWM)

The higher the voltage of SFS pin is, the larger the driving duty is. So, the driving current increases softly according to the increment of SFS level, as shown in Fig.1.

This function is available not only in IC booting but in restart from lock protection.

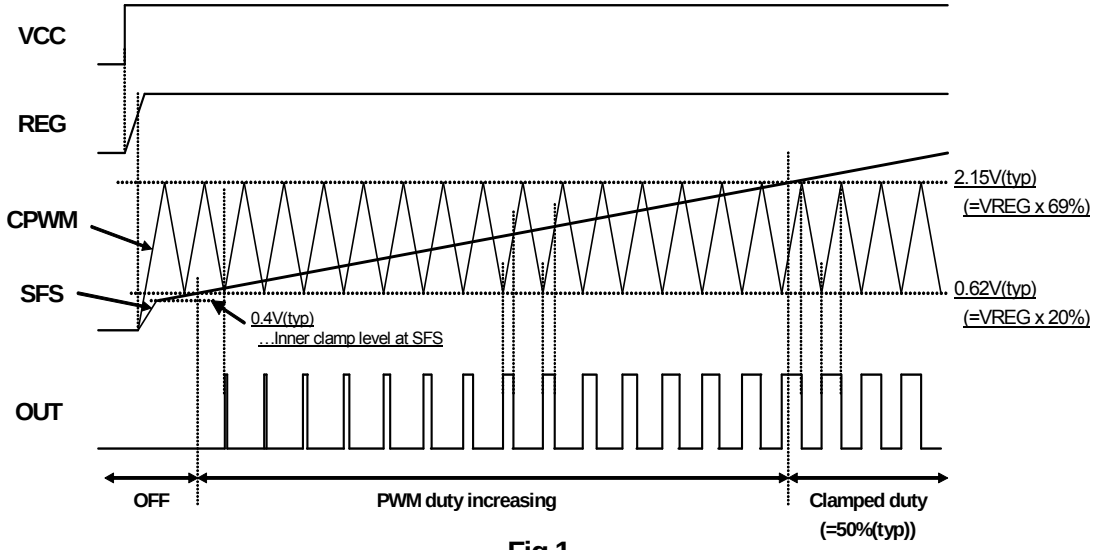


Fig.1

The motor should begin to rotate by the increment of driving duty. After 8th FG edge from IC booting or restart, the control of PWM duty in outputs swithes from SFS level to VTH level, as shown in Fig.2.

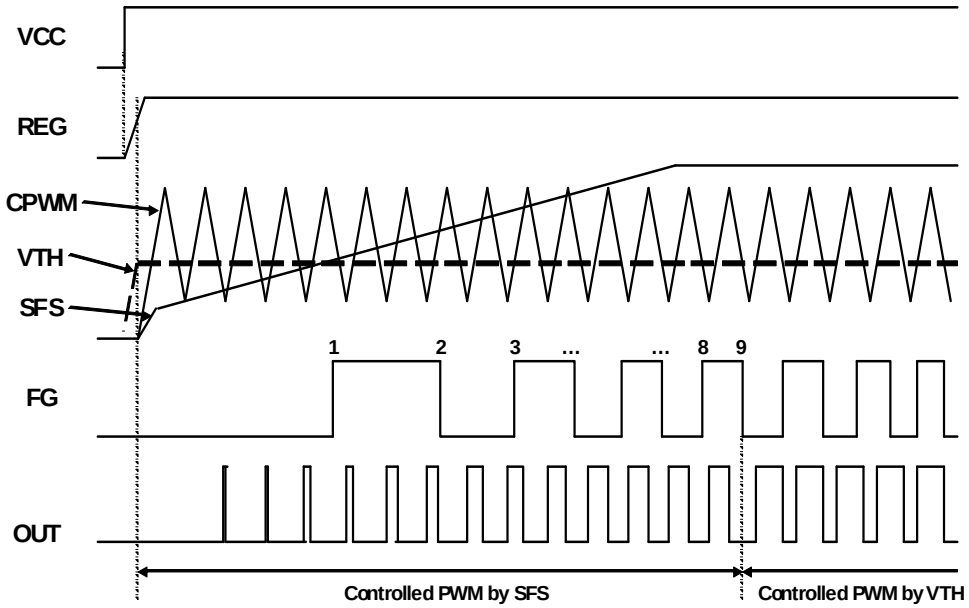


Fig.2

- PWM duty control

Duty of PWM output is determined by comparison of CPWM oscillation and DC level which is input to VTH pin.

PWM output is in the mode of ...

Driving (under the condition of CPWM > VTH)

Regenerating (under the condition of CPWM < VTH)

The minimum duty of PWM output is determined by comparison of CPWM oscillation and DC level which is input to RMI pin.

High duty of PWM output is determined by ...

VTH level (under the condition of RMI > VTH)

RMI level (under the condition of RMI < VTH)

That is, high duty of PWM output decreases only to the one which is determined by RMI level.

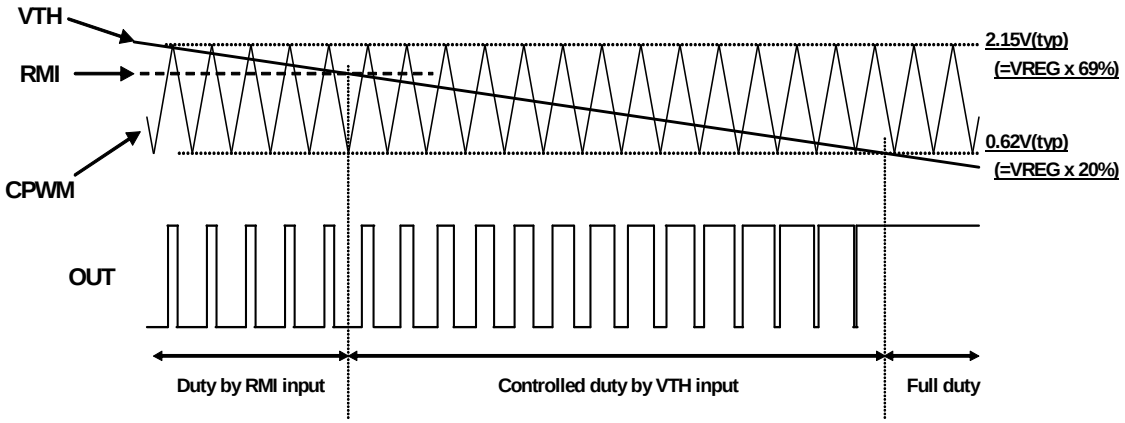


Fig.3

- Soft switching

This IC operates to switch the driving phase of output softly by changing PWM duty gradually, which is called Soft switching.

The term of Soft switching is 18.75% of FG half cycle each before and after the time of phase switching, as shown in Fig.4 with details.

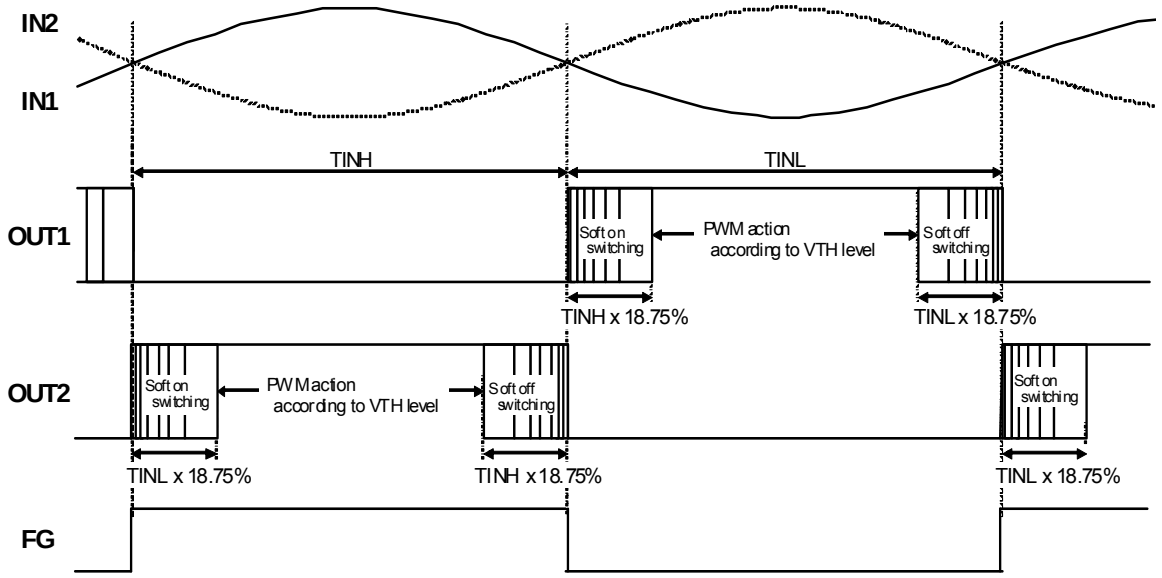


Fig.4

In case that output turns from PWM operation to constant low side driving, PWM high duty decreases by 12.5% of actual duty every 12.5% of Soft switching term, as shown in Fig.5.

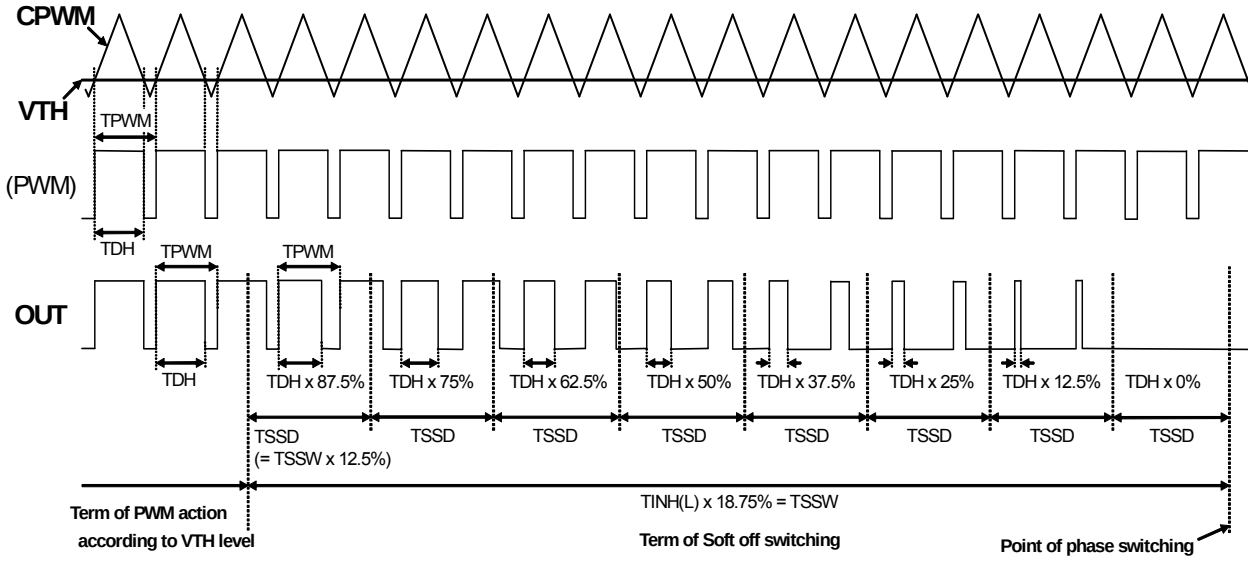


Fig.5

Similarly in case that output turns from constant low side driving to PWM operation, PWM high duty increases by 12.5% of actual duty every 12.5% of Soft switching term. However fixed regenerating term is inserted in 300 usec(typ) after phase switching, as shown in Fig.6.

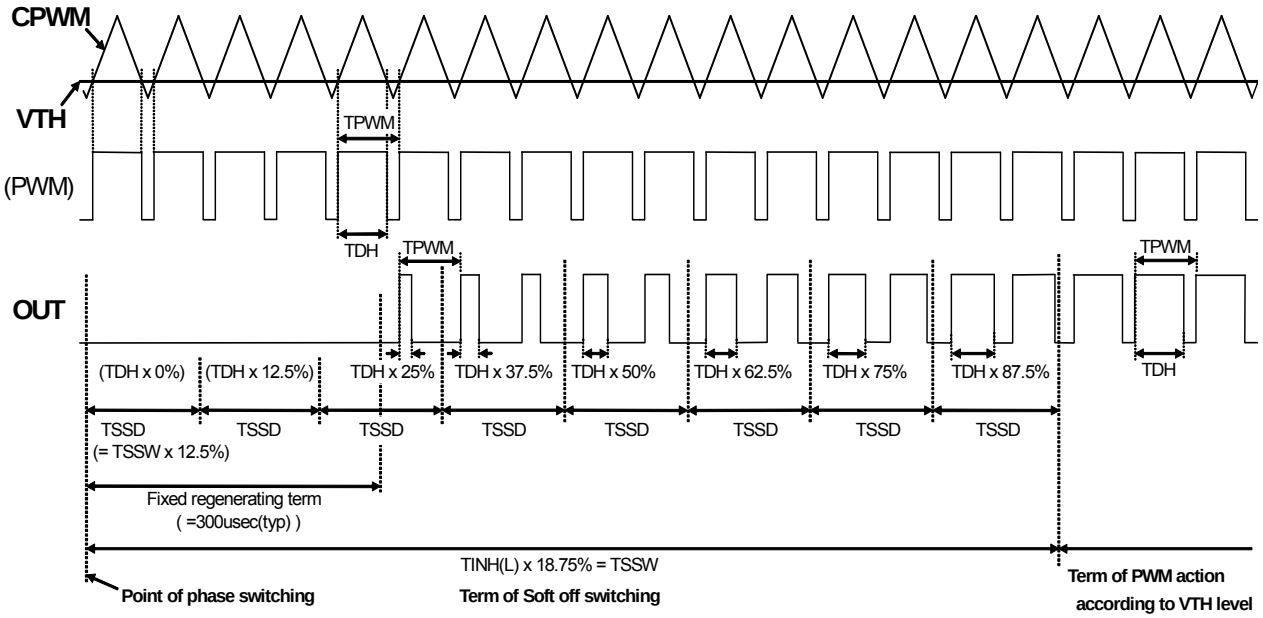


Fig.6

- Lock protection and Auto restart

In case that the motor is locked, this IC operates to protect the motor from the damage by constant large current.

If the crossing of each hall signals isn't detected within a specified period of time, motor driving is cut by turning off the output of high side driving.

After a specified time from turning off the output, IC retries to operate in Start-up mode, as shown in Fig.7.

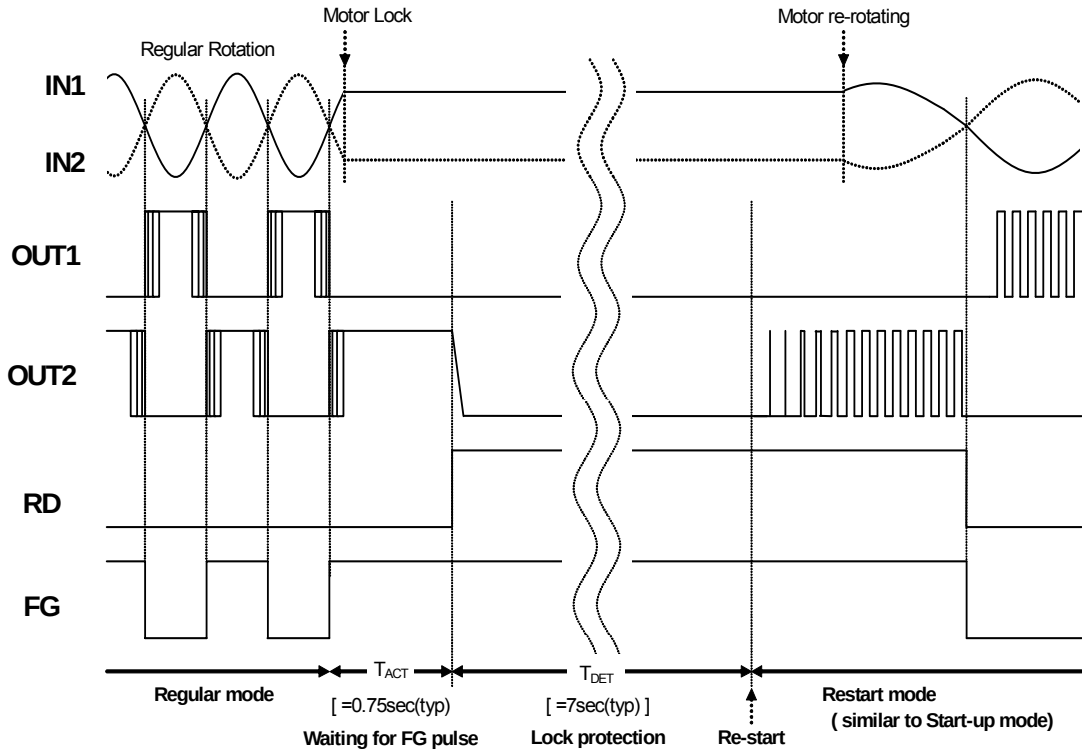


Fig.7

- Others

This IC has protective functions which are Under Voltage Lock Out (UVLO) and Over Voltage Protection (OVP).

The active level of UVLO is under 2.9V (typical) at VCC and the return level is over 3.1V (typical). If UVLO is active, Both of OUT1 and OUT2 are under sleep mode.

The active level of OVP is over 19.8V (typical) at VCC and the return level is under 17.8V (typical). If OVP is active, high side of OUT1 and OUT2 is into sleep but low side keeps on operating according to input signals.

Application Circuit Example

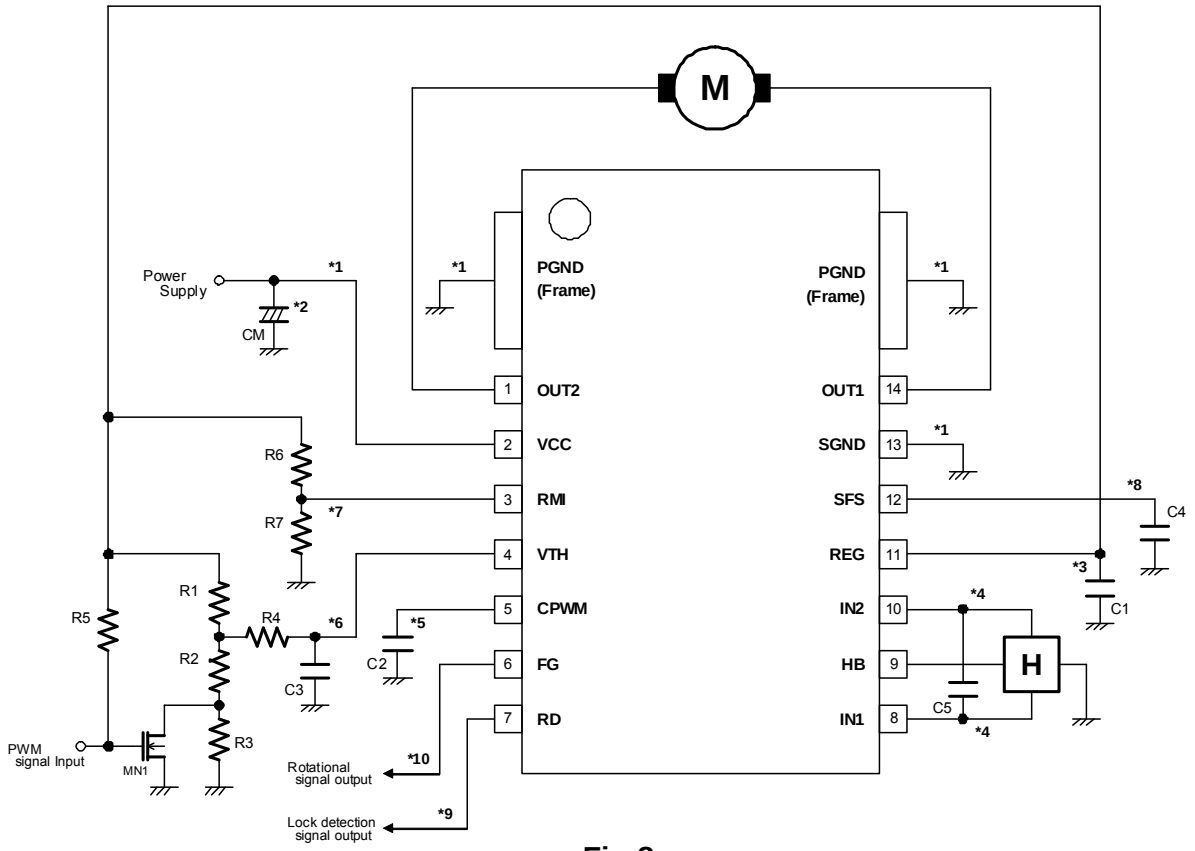


Fig.8

*1 < Wiring of VCC and GND >

PGND (Frame) is connected to power MOSFETs and SGND is to internal circuits. Wiring of those should be separated each other to stabilize SGND by cutting out the influence of the switching noise of power FETs. In the event that external parts for IC are connected to GND, it should be done with SGND.

In addition, PGND (Frame) pins are effective for heat radiation. Therefore, the larger the wiring area of PGND is, the greater the effect is. Considering heat radiation along with the switching noise, the wiring of PGND should be widened as much as possible.

Similarly to PGND, the wiring of VCC should be widened and shortened for suppressing the noise.

*2 < Capacitor for power stabilization >

The capacitor for power stabilization should be enough value to ensure a stable operation. Of course, this capacitor must not be removed.

Under the condition that the value of coil inductance is larger or the value of coil resistance is smaller, the current ripple grows further. Under that condition, it should use the capacitor with larger value to absorb this current ripple. If cannot by capacitor, it must use power-clamp with zener diode.

This capacitor should be set as close to VCC pin and PGND pin as possible.

*3 < Capacitor for stabilization of REG output voltage >

REG output voltage is the regulated voltage as power supplier to inner control circuits. Therefore, it is necessary to stabilize by using a capacitor with enough value for preventing inner control circuits from false operation.

*4 < Hall signal input >

To defend signals against the noise, it is necessary to wire as short as possile from hall sensor to each pin and to conect the capacitor between IN1 and IN2, as shown in Fig.1. Value from 1,000pF to 10,000pF is recommended for C5 in Fig.1. But its value should be selected in consideration with the actual motor action.

$$f_{CPWM} = \frac{1}{2} \times \frac{I_{CPWM}}{C_2 \times (V_{CPH} - V_{CPL})}$$

In the case C_2=100[pF];

$$f_{CPWM=100\,pF} = \frac{1}{2} \times \frac{25.0E^{-6}}{100E^{-12} \times (2.15 - 0.62)} = 81.70[kHz]$$

This is the result which is calculated by typical values of each electrical characteristic in this IC. Actually, there is variability which is defined by min/max in electrical characteristics. In addition, there may be some difference between calculated value and actual value because of a parasitic capacitance on the board and so on.

Therefore, the value of C2 should be settled with actual operation, in view of those factors.

The amplitude of each hall signal must be more than 60mVp-p because of the sensitivity of inner circuit.

*5 < Capacitor to adjust the PWM frequency >

The oscillation for PWM control is generated by connecting a capacitor between CPWM pin and GND. The frequency of this oscillation is calculated as below;

*6 < Input to VTH pin >

VTH pin needs to be input DC signal which is from 0V to VREG.

If the external control signal is the pulse type, it should be flatten by the filter and be shifted to suitable level, shown in Fig.1, to input to VTH pin.

In the case that the high duty of PWM signal input in Fig.1 is D [%], VTH input level flatten by the filter is calculated apprpximately as below;

$$VTH = V_{REG} \times \left\{ \frac{R_2 + R_3}{R_1 + R_2 + R_3} - \frac{R_1 \times R_3}{(R_1 + R_2 + R_3) \times (R_1 + R_2)} \times \frac{D}{100} \right\}$$

This calculation is justified by the condition that Rds of MN1 << R3. So, a large value of resistor should be selected to R3.

But, too large value of R1 – R3 and R4 causes the instability because of the effect of input impedance at VTH pin.

The recommendation value of R1 – R3 and R4 is from 4.7k[ohm] to 47k[ohm].

The cut-off frequency fc by C3 and R4 is calculated as below;

$$f_c = \frac{1}{2\pi \times C_3 \times R_4}$$

The actual value of C3 or R4 is better to select more than 50 times the above calculation value to be flatten thoroughly. Furthermore, it is better to do it by the value of C3 because of the effect of input impedance at VTH pin.

To compensate for disconnection of PWM input, it is recommended that the gate of the FET is pulled up to REG with a resistor as R5 shown in Fig.1.

*7 < Adjustment of the minimum duty of PWM output >

As for the way of RMI input, the divided voltage of REG by resistors, as R6 and R7 shown in Fig.1, is recommended. In addition, it would be better to use a resistor which the value is from 4.7k[ohm] to 47k[ohm], in view of impedence at RMI pin.

If not use this pin, it should be shorted to VTH pin.

*8 < Adjustment of soft starting >

The time T_{SFS} from IC booting to coming up to clamped duty is calculated apprpximately as below;

$$T_{SFS} = \frac{C_4 \times (V_{CPH} - V_{SFSCL})}{I_{SFS}}$$

The value of C4 should be selected in consideration with the start-up characteristic of motor and the time of lock detection.

*9 < RD output >

RD output is N-ch MOSFET with the opened drain. It is “Low level” in motor rotation and “High impedance” in lock detection.

If not use, this pin would be better to open.

*10 < FG output >

FG output is N-ch MOSFET with the opened drain. It is the rotational signal made by the hall signal input.

If not use, this pin would be better to open.

Mouser Electronics

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